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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

BEREZNY, NEAL

ART UNIT PAPER NUMBER

2823

DATE MAILED: 05/21/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/516,653

Applicant(s)

DOYLE, BRIAN

Examiner

Neal Berezny

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 February 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-28 and 39-47 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-28 and 39-47 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☒ The proposed drawing correction filed on 22 February 2002 is: a) ☒ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 19-21 and 26-28 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. It is claimed that an etch results in an SOI structure, which is not clear how this is accomplished either in the claims or the specifications.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-6, 9-16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chapple-Sokol et al. (5,612,255). Chapple-Sokol teaches patterning a first oxide, fig.1A, el.102, forming poly spacers, fig.1B, el.106, by means of RIE, col.2, ln.55, forming a plurality of channels, fig.1C and 1D, el.106 and 116, forming a gate oxide, fig.2C, el.122, col.3, ln.30-32, forming a gate over the channels, fig.2C, el.124,

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col.3, ln.33-35, in which each channel is a one dimension quantum wire, col.3, ln.60-65. Further, Chapple-Sokol teaches the formation of sources, drains, and contacts, el.132, 134, and 136, col.3, ln.47-51, and anticipates the usage of various isolation mechanisms well known in the art, such as use of a SOI substrate, dopant under the trench, and insulator filled trenches, col.3, ln.38-43, and would be obvious for one skilled in the art to employ such processes into the teachings of Chapple-Sokol.

5. Chapple-Sokol does not teach the practice of forming spacers on spacers to further reduce the size of the quantum wire even further. It would be obvious to one skilled in the art to merely duplicate the Chapple-Sokol process twice to further reduce the width of the wire. It has been held that a mere duplication of part or processes involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.

6. Chapple-Sokol also appears not to specifically state the use of a nitride spacer mask instead of the poly spacer mask. In terms of spacer masks, nitride and poly are well known to be equivalent materials and it would be obvious to one skilled in the art to substitute one for the other and provide for greater process latitude.

7. Official notice is given that triple gate FET's are well known in the art and it would be obvious to employ multiple gate FET technology to Chapple-Sokol's quantum wire FET to provide for multiple inputs into the switching device and therefore enhance the capabilities of the device.

8. Claims 7-8, 17, 19-28, and 39-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chapple-Sokol as applied to claims 1-6,9-16, and 18 above, and further in view of Kendall, (Kreidl Memorial Lecture, Oct. 30, 1995). Kendall teaches the

art of quantum wire arrays and related geometries employing studs less than 5nm in width, last par. on page 1. Chapple-Sokol also teaches various geometries of their quantum wires, see col.3. It would be obvious to one of ordinary skill in the art to employ the claimed geometries in the teachings of both Chapple-Sokol and Kendall. It has been held that mere changes in dimensions to be within the level of one of ordinary skill in the art. *In re Rose*, 105 USPQ 237 (CCPA 1955). Further, applicant has failed to disclose the critical nature or unexpected results arising there from. One would be motivated to combine the teachings of Kendall with Chapple-Sokol in order to reduce the geometries of the QWFET to increase both performance and density of devices.

Specifications

9. The amendment filed 2/22/02 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows:

A. Amendment of p.2, ln.6, changes silicon to semiconductor, which broadens the specifications.

B. Amendment of p.8, beginning at ln.2 introduces limitations, plurality of channels and quantum wire, into the description of figure 1f, broadening the specifications, as originally presented.

C. Amendment of p.8, beginning at line 17, introduces additional dimensional limitations, X, P, and W, into the paragraph.

D. Amendment of p.10, beginning at line 7, introduces an additional variable, X, into the paragraph, broadening the specifications.

E. Amendment of p.10, beginning at line 17, changes the aspect ratio discussion from the quantum wire to the second nitride spacer mask. Also additional steps are included in the discussion of the process related to the structure of fig.4.

F. Amendment of p.13, beginning at line 8, includes additional steps to the original discussion of the process related to the structure of fig.7.

G. Amendment of p.14, beginning at line 1, changes the role of figure 10 from being **the inventive method to an inventive embodiment**. It changes the scope of the flow diagram from being the critical process flow of the entire invention to just one embodiment of several.

Applicant is required to cancel the new matter in the reply to this Office Action.

Response to Arguments

10. Applicant's amendment of the claims, were successful in overcoming examiner's rejection of claims 16-21 under 35 USC 112, par.1, and claims 19-21 under 35 USC 112, par.2.

11. Applicant's arguments filed 2/22/02 have been fully considered but they are not persuasive. Applicant traverses examiner's 112, par.1 rejection of claims 19-21 and 26-28. Applicant's argument is unclear, but seems to be related to a possible difference in semantics, SOI structure vs. SOI topology, and reference to figures in the specifications that may involve SOI structure or topology. Applicant appears to be overlooking the fact

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that the claims are being rejected and not the specification. What is at issue is whether the invention as **claimed** is supported by the specifications. The structure **claimed** appears not to form an SOI structure as a result of an etch. Therefore, one of ordinary skill would need to rely on the specifications for instructions, but the material cited by applicant does not enable one to build an SOI topology from the **claimed** structure. Applicant's attempt to extrapolate the forming of an SOI topology from unclaimed structures to claimed structures is vague and indefinite, nor supported by the specifications.

12. Applicant argues examiners 103 rejection of claims 1-6, 9-16, and 18 on the grounds that a prima facie case has not been made. Applicant makes this assertion on the grounds that a mere duplication of parts or process steps is somehow invalid because the second set of duplicated process steps involves new elements, and the Chapple-Sokol reference refers to a final structure that somehow precludes reasonable expectation of success, and that Chapple-Sokol does not specifically teach the second set of steps for the second set of spacers. These arguments fail to overcome the prima facie case made because they attack the general principal of a 103 rejection and the general issue of obviousness of duplicated steps. Examiner agrees that a second set of steps, for any process, must by definition include a new set of elements, which are similar to or duplicates of the first set, but that does not mean that they are "new" elements in the context *St. Regis*. In addition, the premise of all 103 rejections is that a reference is "lacking" in one or more elements, so that, by itself, does not constitute

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insufficient grounds for a prima facie case. Further, since most 103 rejections are modifications of a final product, applicant's "final structure" argument is frivolous.

13. In conclusion, a valid prima facie case has been made and applicant's arguments do not support examiner's withdrawal of the rejection. Examiner suggests that applicant try to overcome the rejection by elaborating on those aspects of the claimed invention that require special considerations or unexpected results, which would demonstrate the non-obviousness of the second set of process steps.

14. Applicant also traverses examiner's assertion that as masking materials, nitride and poly are equivalent materials. Applicant argues that the etch recipes for the two are very different. That may well be true, but irrelevant because these materials have been used as masks and etched so extensively, that anyone of ordinary skill would know how to etch both materials. In addition, the issue is not how they etch but rather how well do they function as **masks**.

15. Applicant traverses examiner's assertion that triple-gate FETs are well known, but then admits that they are well known in the art, see p.16, middle of last paragraph. Applicant argues that the claimed method as a whole is not taught by the Chapple-Sokol reference, but that is the whole point behind a 103 rejection.

16. Applicant argues the examiner's 103 rejection based on the combination of Chapple-Sokol and Kendall. Applicant asserts that Kendall's geometries are vague and indefinite because of the term "several micrometers high" and refers to different processes. Neither assertion is correct because Kendall describes a process for the formation of quantum wires, as does applicant, but for a different electrical purpose. In

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response to applicant's nonanalogous art argument, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, the process of forming quantum wires and not necessarily the application of those wires.

17. Regarding applicant's vague and indefinite argument, examiner would like to point out that the rules regarding claim language are very different from text found in articles and the specifications. The phrase "several micrometers high conveys enough information and understanding to be used to anticipate applicant's invention.

18. In addition applicant argues dimensional ratios and pitch, and then challenges examiner's motivation to combine so as to reduce geometries for the purpose of increasing performance and density. Applicant employs only the worst case differences in geometries, when it is the best case comparisons that rejections must address to insure that the claims do not infringe the prior art. Applicant is cautioned in this argument and previous ones, that a lack of disclosure in the specifications of the critical nature of a particular element has a presumed assumption that applicant considers the nature of such elements as obvious, which is why it would not need to be fully described in the specifications.

19. Finally, applicant's assertion that there is no support for the motivation to reduce geometries in the prior art, and **only** found in the applicant's disclosure, is frivolous. Is applicant actually saying that the applicant is the first to think of reducing geometries in

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order to increase performance and density of electronic devices? Are we to conclude that Moore's law, as observed over decades, has not been a deliberate effort to reduce geometries, but some sort of random phenomena? Does applicant really want the examiner to produce a reference that describes the motivation to reduce size, which has strongly driven the entire semiconductor and electronic industry for decades?

CONCLUSION

20. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).


A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

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21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Neal Berezny whose telephone number is (703) 305-1481. The examiner can normally be reached on Monday to Friday from 9:00 to 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached at (703) 308-4918. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.


George Fourson
Primary Examiner
2823

 5/20/02

Neal Berezny

Patent Examiner

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